112 Rejection

Claims 1-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention. The Applicant respectfully requests the withdrawal of this rejection based on the following remarks.

As it regards Claim 4, the Applicant respectfully disagrees with the Examiner's contention that there is no connection between the "constant ramp generator" of this Claim and the circuit of Claim 1. The constant ramp generator of Claim 4 is related as a building block component of the circuit for controlling a rise time of a signal as is set forth in Claim 1. The limitations of Claim 4 that recite this component serve to further define the circuit of Claim 1.

As it regards Claim 6, it should be appreciated that "given" is employed to mean "particular" which is a normal usage of the term.

As it regards Claim 7, the Applicant respectfully disagrees with the Examiner's contention that there is no connection between the "level shifter" of this Claim and the circuit of Claim 1. The level shifter of Claim 4 is related as a building block component of the circuit for controlling a rise time of a signal as is set forth in Claim 1. The limitations of Claim 7 that set forth this component serve to further define the circuit of Claim 1.

As it regards Claim 8, the Applicant respectfully disagrees with the Examiner's

contention that there is no connection between the "two non overlapping clock signals" of this Claim and the circuit of Claim 1. The two non overlapping clock signals of Claim 8 are generated and supplied to the circuit by structure 103 (see Figure 1) in a manner that is fully discussed in the Applicant's specification. The limitations of Claim 7 that set forth this component serve to further define the circuit of Claim 1.

As it regards Claims 11 and 12, the Applicant respectfully disagrees with the Examiner's contention that the recited comparator of these Claims does not perform a feedback function. The operation of the comparator in the context of the feedback operation of the Applicants disclosed circuit is fully described at page 8, lines 1-14 of the Applicant's specification.

As it regards Claim 13, the Applicant respectfully disagrees with the Examiner's contention that there is no connection between the "divide by N counter" of this Claim and the circuit of Claim 1. The divide by N counter of Claim 13 is related as a building block component of the circuit for controlling a rise time of a signal as is set forth in Claim 1. The limitations of Claim 13 that set forth this component serve to further define the circuit of Claim 1.

As it regards Claim 20, the Applicant respectfully disagrees with the Examiner's contention that the limitations of Claim 20 are not defined. The Applicant fully discusses the recited programming voltage at page 7, lines 20-27.

103 Rejection

Claims 1, 2, and 6-12 are rejected under 35 U.S.C. 102(b) as being unpatentable over Kazerounian et al. The Applicant has reviewed the cited references and respectfully submits that the present invention as recited in Claims 1, 2 and 6-12 is neither shown nor suggested by Kazerounian et al.

The Examiner is respectfully directed to independent Claim 1 which recites that an embodiment of the present invention is directed to a method for controlling a rise time of a signal, comprising:

> a switched capacitor circuit coupled to said voltage multiplication circuit which controls said output voltage from said voltage multiplication circuit which controls said output voltage from said voltage multiplication circuit, wherein a ratio between a first capacitor of said switched capacitor circuit and a second capacitor of said switched capacitor circuit determines said rise-time of said signal, said circuit for controlling a rise time of a signal further comprises a constant ramp generator.

Dependent Claims 2 and 6-12 depend from independent Claim 1. These Claims recite further features of the present invention.

Kazerounian et al. does not anticipate or render obvious a circuit for controlling a rise time of a signal wherein "said circuit for controlling a rise time of a signal further comprises a constant ramp generator". By contrast, the Kazerounian et al. reference only discloses an on chip high voltage generator and regulator in an integrated circuit package. It should be appreciated that the sub circuit components that constitute the high voltage

generator and regulator of Kazerounian et al. are shown in the Kazerounian et al. reference at Figure 2. However, nowhere in the Kazerounian et al. reference, including in Figure 2 and it's accompanying discription is a circuit for controlling a rise time of a signal that comprises a constant ramp generator such as is set forth in Claim 1 shown or taught. Consequently, Kazerounian et al. does not show or suggest the Applicant's invention as it is set forth in Claim 1.

Therefore, the Applicant respectfully submits that Kazerounian et al. does not anticipate or suggest the present claimed invention as is recited in Claim 1 and, as such, Claim 1 traverses the Examiner's basis for rejection under 35 U.S.C. §102(b). Accordingly, the Applicant respectfully submits that Claim 1 is in condition for allowance. In addition, the Applicant respectfully submits that Kazerounian et al. does not anticipate or suggest the present invention as is recited in Claims 2 and 6-12 dependent on Claim 1, and that these Claims are also in condition for allowance as being dependent on an allowable base claim.

SUMMARY

In view of the foregoing amendments and remarks, Applicants respectfully submit that the pending claims are in condition for allowance. Applicants respectfully request reconsideration of the application and allowance of the pending claims.

If the Examiner determines the prompt allowance of these claims could be facilitated by a telephone conference, the examiner is invited to contact Reginald A. Ratliff at (408) 938–9060.

Respectfully submitted,

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Dated: 1/23, 2003

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MARKED UP VERSION TO SHOW CHANGES MADE

IN THE CLAIMS

Please cancel Claim 4.

Please amend Claims 1 and 14 as follows:

1. (Amended) A circuit for controlling a rise-time of a signal, comprising:

a voltage multiplication circuit which converts an input voltage to an output voltage greater than said output voltage;

a switched capacitor circuit coupled to said voltage multiplication circuit which controls said output voltage from said voltage multiplication circuit, wherein a ratio between a first capacitor of said switched capacitor circuit and a second capacitor [of said switched capacitor circuit] determines said rise-time of said signal, said circuit for controlling a rise time of a signal further comprises a constant ramp generator.

14. (Amended) A switched capacitor controller for controlling a rise time of an on-chip generated voltage source, comprising:

a charge pump;

a ramp generator coupled to said charge pump, wherein said ramp generator comprises a switched capacitor [a switched capacitor coupled to said ramp generator];

a regulator circuit coupled to said switched capacitor circuit which causes a capacitor to switch between ground and a node, wherein a stair-step ramp signal is generated and said rise time is controlled according to said switched capacitor.